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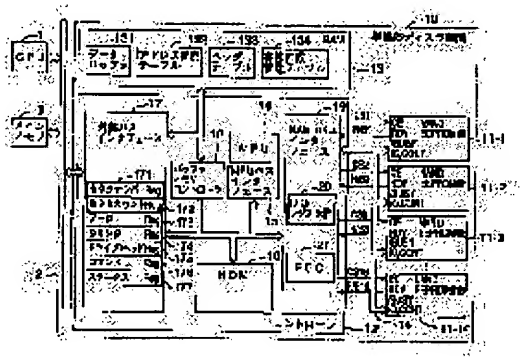
(54) SEMICONDUCTOR DISK DEVICE

(57)Abstract:

PURPOSE: To improve the write access speed to a flush EEPROM.

CONSTITUTION: A NAND bus interface 19 receives 16 ready/busy signals from flush EEPROMs 11-1-11-16 independently and manages the operating state of each flush EEPROM. Thus, a flush EEPROM being a write access object is ready without awaiting the end of operation of all the flush EEPROMs 11-1-11-16 and the write access to the flush EEPROM being the write access object is started. Furthermore, since each flush EEPROM is of a command control type in which the write operation is automatically executed, it is possible to make write access to other flush EEPROM while a flush EEPROM is in data write state and then the plural flush EEPROMs are operated in parallel.



LEGAL STATUS

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